Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (previously presented): In a processor, a method for performing computer graphics calculations, said method comprising:

representing a vertex in a computer graphics image with a plurality of coordinates;

transforming said plurality of coordinates into a plurality of transformed coordinates; and

using a floating point magnitude compare instruction to perform a magnitude comparison between at least a portion of said plurality of transformed coordinates and a value representing a plurality of edges of a specified view volume, wherein comparison results for at least three view volume edges are obtained.

Claim 2 (original): The method for performing computer graphics calculations as recited in Claim 1 wherein said portion of said plurality of transformed coordinates are processed in parallel.

Claim 3 (original): The method for performing computer graphics calculations as recited in Claim 1 further comprising:

setting a plurality of condition code bits to one or more specific states to indicate results of said magnitude comparison.

Claim 4 (original): The method for performing computer graphics calculations as recited in Claim 1 further comprising:

specifying a compare condition in said floating point magnitude compare instruction.

Claim 5 (original): The method for performing computer graphics calculations as recited in Claim 4 further comprising:

setting one of said plurality of condition code bits to indicate true if an associated compare condition is true and setting said one condition code bit to indicate false if said associated compare condition is false.

Claim 6 (original): The method for performing computer graphics calculations as recited in Claim 1 further comprising:

converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

Claim 7 (original): The method for performing computer graphics calculations as recited in Claim 6 wherein said first convert instruction is a CVT.PS.PW instruction.

Claim 8 (original): The method for performing computer graphics calculations as recited in Claim 1 further comprising:

converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

Claim 9 (original): The method for performing computer graphics calculations as recited in Claim 8 wherein said second convert instruction is a CVT.PW.PS instruction.

Claim 10 (original): The method for performing computer graphics calculations as recited in Claim 1 wherein said floating point magnitude compare instruction is a CABS instruction.

Claim 11 (original): A processor for computer graphics calculations, said processor comprising:

a bus;

an instruction dispatch unit coupled to said bus, said instruction dispatch unit for dispatching instructions to a floating point unit; and

said floating point unit coupled to said bus, said floating point unit for executing said instructions to implement a method for performing computer graphics calculations, said method comprising:

representing a vertex in a computer graphics image with a plurality of coordinates;

transforming said plurality of coordinates into a plurality of transformed coordinates; and

using a floating point magnitude compare instruction to perform a magnitude comparison between at least a portion of said plurality of transformed coordinates and a

value representing a plurality of edges of a specified view volume, wherein comparison results for at least three view volume edges are obtained.

Claim 12 (original): The processor of Claim 11 wherein said method for performing computer graphics calculations further comprises:

setting a plurality of condition code bits to one or more specific states to indicate results of said magnitude comparison.

Claim 13 (original): The processor of Claim 11 wherein said method for performing computer graphics calculations further comprises:

specifying a compare condition in said magnitude compare instruction.

Claim 14 (original): The processor of Claim 13 wherein said method for performing computer graphics calculations further comprises:

setting one of said plurality of condition code bits to indicate true if an associated compare condition is true and setting said one condition code bit to indicate false if said associated compare condition is false.

Claim 15 (original): The processor of Claim 11 wherein said method for performing computer graphics calculations further comprises:

converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

Claim 16 (original): The processor of Claim 15 wherein said first convert instruction is a CVT.PS.PW instruction.

Claim 17 (original): The processor of Claim 11 wherein said method for performing computer graphics calculations further comprises:

converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

Claim 18 (original): The processor of Claim 17 wherein said second convert instruction is a CVT.PW.PS instruction.

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Claim 19 (original): The processor of Claim 11 wherein said floating point magnitude compare instruction is a CABS instruction.

Claim 20 (currently amended): In a system including a general purpose processor and a memory, a method for comparing a plurality of floating point values comprising:

storing a first instruction in said memory, wherein said first instruction is formatted to operate on a plurality of operands;

dispatching said first instruction to said general purpose processor; and

executing said first instruction in said general purpose processor, wherein said processor operates on said plurality of operands in parallel to perform a plurality of magnitude compare operations, and wherein each magnitude compare operation involves a single comparison.

Claim 21 (original): The method of claim 20 further comprising:

setting a plurality of bits, wherein each of said plurality of bits is set by said first instruction to a particular state to indicate a result of one of said plurality of magnitude compare operations.

Claim 22 (original): The method of claim 21 wherein said first instruction is part of a general purpose instruction set architecture.

Claim 23 (original): The method of claim 21 wherein said first instruction is part of an application specific extension to a general purpose instruction set architecture.

Claim 24 (original): The method of claim 21 wherein said plurality of bits as set by said first instruction indicate whether a graphics primitive will cross at least one edge of a view volume.

Claim 25 (original): The method of claim 21 wherein said plurality of bits as set by said first instruction indicate whether a graphics primitive will cross at least three edges of a view volume.

Claim 26 (original): The method of claim 25 wherein said first instruction is executed in a single clock cycle.

Claim 27 (currently amended): In a processor, a method comprising:

dispatching a single instruction to an execution unit, said single instruction being formatted to operate on a plurality of operands;

providing said plurality of operands to said execution unit, wherein said plurality of operands represent a plurality of view volume edges of a given view volume; and

executing said single instruction which causes said execution unit to perform a plurality of magnitude compare operations in parallel on said plurality of operands, said operations testing at least three view volume edges of said given view volume, wherein each magnitude compare operation involves a single comparison.

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Claim 28 (original): The method of claim 27 further comprising setting a plurality of bits, said bits indicating whether said at least three view volume edges have been crossed by a graphics primitive.

Claim 29 (original): The method of claim 28 wherein said plurality of operands are in a paired-single data format.

Claim 30 (currently amended): In a system including a general purpose processor and a memory, a method comprising:

storing an instruction in said memory;

dispatching said instruction to said general purpose processor;

executing said instruction which causes said general purpose processor to perform a first magnitude compare operation between a first and a second operand, wherein said first magnitude compare operation involves a single comparison.

Claim 31 (original): The method of Claim 30 wherein said instruction is formatted to operate on a plurality of operands.

Claim 32 (original): The method of claim 31 wherein said executing includes causing said general purpose processor to perform a second magnitude compare operation between a third and fourth operand.

Claim 33 (original): The method of Claim 32 wherein said first and second magnitude compare operations are carried out in parallel.

Claim 34 (original): The method of Claim 33 further comprising:

setting a plurality of bits, wherein each of said plurality of bits is set to a particular state to indicate a result of one of said first or second magnitude compare operation.

Claim 35 (original): The method of Claim 33 wherein said second and fourth operands have the same magnitude.

Claim 36 (original): The method of Claim 34 wherein said instruction is part of an application specific extension to a general purpose instruction set architecture.

Claim 37 (original): The method of Claim 34 wherein said instruction is part of a general purpose instruction set architecture.

Claim 38 (currently amended): A computer program product comprising a computer-readable medium having a plurality of instructions stored thereon, the plurality of instructions for enabling a general purpose processor to perform certain operations, wherein the plurality of instructions includes:

a first instruction that enables the general purpose processor to process a first plurality of operands in accordance with a first method, said first method comprising:

performing a plurality of magnitude compare operations on said first plurality of operands in parallel; and

setting a plurality of bits to one or more specific states to indicate results of said plurality of magnitude compare operations,

wherein each magnitude compare operation involves a single comparison.

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Claim 39 (original): The computer program product of Claim 38 wherein said plurality of instructions further comprises a second instruction that converts a second plurality of operands from a plurality of fixed point values into a plurality of floating point values, wherein said floating point values are in a paired-single data format.

Claim 40 (original): The method for performing computer graphics calculations as recited in Claim 1 wherein said plurality of coordinates and said plurality of transformed coordinates are in a paired-single data format.

Claim 41 (original): The processor of Claim 11 wherein said plurality of coordinates and said plurality of transformed coordinates are in a paired-single data format.